



First Named
Inventor : Kurt Kimber et al.
Appln. No. : 10/616,801
Filed : July 10, 2003
Title : SYSTEM AND METHOD FOR DYNAMIC ESD
PROTECTION
Docket No. : P440.12-0006

Group Art Unit:
Examiner:

INFORMATION DISCLOSURE STATEMENT

Commissioner For Patents
P.O. Box 1450
Alexandria, VA 22313-1450

I CERTIFY THAT THIS PAPER IS BEING SENT BY U.S. MAIL,
FIRST CLASS, TO THE ASSISTANT COMMISSIONER FOR
PATENTS, WASHINGTON, D.C. 20231, THIS 3 DAY OF

October, 2003.

David R. Fairbairn
PATENT ATTORNEY

Sir:

The enclosed PTO Form-1449 lists patents and publications submitted pursuant to 37 C.F.R. 1.97. Copies of the patents or publications are enclosed as necessary [if application filing date is after June 30, 2003, copies of U.S. patents and application publications are not required].

TIME OF FILING

The Information Disclosure Statement is being filed:

1. X with the application or within three months of the filing date of a national application (other than a continued prosecution application under 37 C.F.R. 1.53(d)) or date of entry into the national stage of an international application or, to the best of the undersigned's knowledge, before the mailing date of a first Office action on the merits or a first office action after the filing of a request for continued examination under 37 C.F.R. 1.114, whichever event occurs last. In accordance with 37 C.F.R. 1.97(b), no certification or fee is required.

Respectfully submitted,

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LIST OF PATENTS AND PUBLICATIONS FOR
APPLICANT'S INFORMATION
DISCLOSURE STATEMENT

U.S. PATENT DOCUMENTS

Examiner Initials	Document No.	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Documents
AA	6,429,489	08-06-2002	Botula et al.
AB	6,549,061	04-15-2003	Voldman et al.
AC			
AD			
AE			
AF			
AG			
AH			
AI			
AJ			
AK			

FOREIGN PATENT DOCUMENTS

	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Documents	Translation Yes No
AL				
AM				
AN				

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

AO	"An On-Chip ESD Protection Circuit with Low Trigger Voltage in BiCMOS Technology", Albert Z. H. Wang and Chen-Hui Tsay, <i>IEEE Journal of Solid-State Circuits</i> , Vol. 36, No. 1, January 2001.
AP	
AQ	

EXAMINER:

DATE CONSIDERED:

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.